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EXAMINER	
KIM, DANIEL Y	

ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 10/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/829,621	LUICK, DAVID ARNOLD	
	Examiner	Art Unit	
	Daniel Kim	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *11 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

10/12/06

STEPHEN C. ELMORE
PRIMARY EXAMINER

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office Action is in response to applicant's communication filed August 11, 2006 in response to the PTO Office Action mailed May 11, 2006. The applicant's remarks and amendments to the claims and/or the specification were considered with the results that follow.

2. In response to the last Office Action, claims 1, 10 and 20 have been amended, andno claims have been canceled or added. Claims 1-20 remain pending in this application.

Response to Arguments

3. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-3, 9-12 and 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hironaka et al (US PGPub No. 20040088489) and Emer et al (US Patent No. 5,933,860).

For claim 1, Hironaka discloses a digital data processing device, comprising:

instruction logic which selects and decodes instructions for execution (a selection circuit which selects one set of data which is required by the processor among sets of data read from a plurality of selected banks through the output port for usual data, par. 0203);

execution logic which executes instructions (each instruction issued from the cache is executed by an execution unit, par. 0132);

a first cache for temporarily storing data, said first cache comprising a plurality of banks, each bank containing at least one respective access port for accessing data in the bank (a multi-port... cache with a plurality of banks, par. 0131); and

wherein said instruction logic selects multiple instructions for concurrent execution, said instruction logic using said bank predict values of said instructions to select multiple instructions which access said first cache for concurrent execution (the multi-port cache simultaneously fetches and issues instructions from a plurality of banks, par. 0131; par. 0146); and

(a) reading data from said first cache, and (b) writing data to said first cache (a multi-port bank memory having a plurality of banks which store instruction data and a plurality of ports; instruction data reading means for reading specified instruction data from the multi-port bank memory as instruction data of an instruction cache, par. 0032).

Hironaka fails to disclose a respective bank predict value is associated with each of said at least some instructions accessing said first cache, each said bank predict value predicting a bank of said first cache to be accessed by its associated instruction.

Emer discloses an instruction cache having a plurality of banks for storing a subset of data from memory, including a prediction mechanism for predicting which bank of the I-cache contains the required data, where a prediction value is associated with each instruction stored in the I-cache and may either be stored with the I-cache data, or in a separate memory included before the I-cache (abstract), and a method and means of addressing a cache memory having a plurality of banks of memory locations includes the steps of determining, responsive to retrieved instruction data, a number of potential next addresses of required data stored in the cache memory and storing, at a location associated with the retrieved instruction data, a prediction value which indicates which one of the banks of the cache memory stores the required data, and is determined responsive to a type of the retrieved instruction data; the method further includes the step of selecting, responsive to said prediction value, one of said potential next addresses for addressing said cache memory (col. 3, lines 33-45, 57-59).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to combine Hironaka and Emer to include bank predict values associated with instructions because they may be used to provide fast and accurate bank prediction during operation (col. 3, lines 60-63), and by incorporating accurate bank prediction, the system incorporates the performance advantages of direct mapped cache addressing with the low miss rates associated with set-associative cache

designs, and the accuracy of the bank prediction is further enhanced because the inherent nature of the stored data is taken into account when formulating the associated bank prediction value (col. 3, lines 63-67, col. 4, lines 1-2), as taught by Emer.

For claim 2, the combined teachings of Hironaka and Emer as per rejection of claim 1 further help disclose a second cache for temporarily storing data, wherein said second cache stores instructions executable by said execution logic and said first cache stores data other than instructions, and wherein said bank predict values are stored in said second cache (Emer: col. 3, lines 33-59).

For claim 3, the combined teachings of Hironaka and Emer as per rejection of claim 1 further help disclose each said bank of said first cache contains a plurality of read ports and at least one write port (Hironaka: a plurality of banks and a plurality of ports including an instruction port unit consisting of at least one port used to have access to an instruction from the parallel processor, and a data port unit consisting of at least one data port used to have access to data from the parallel processor, par. 0028).

For claim 9, the combined teachings of Hironaka and Emer as per rejection of claim 1 further help disclose said digital data processing device is implemented in a single semiconductor chip (Hironaka: fig. 4, item 10).

For claim 10, the combined teachings of Hironaka and Emer as per rejection of the above claims is incorporated herein.

These teachings further help disclose a memory (Hironaka: a main memory which stores programs or various kinds of data or information, par. 0003); and

at least one processor, said processor communicating with said memory over at least one communications path, said processor including instruction logic for selecting and decoding instructions for execution, and execution logic for executing instructions (Hironaka: a processor, par. 0003);

a first cache coupled to said processor and temporarily storing data from said memory, said first cache comprising a plurality of banks, each bank containing at least one respective access port for accessing data in the bank (Hironaka: par. 0131); and

wherein at least some said instructions, when executed by said execution logic, access said first cache to perform at least one of: (a) reading data from said first cache, and (b) writing data to said first cache, and wherein a respective bank predict value is associated with each of said at least some instructions accessing said first cache, each said bank predict value predicting a bank of said first cache to be accessed by its associated instruction (Emer: abstract; col. 3, lines 33-59); and

wherein said instruction logic selects, from among a set of multiple instructions eligible to execute by said execution logic, a subset of multiple instructions for concurrent execution by said execution logic, said instruction logic using said bank predict values of said instructions to select multiple instructions which access said first cache for inclusion in said subset (Emer: abstract; col. 3, lines 33-59).

For claim 11, the combined teachings of Hironaka and Emer as per rejection of claim 10 further help disclose a second cache for temporarily storing data, wherein said second cache stores instructions executable by said processor and said first cache

stores data other than instructions, and wherein said bank predict values are stored in said second cache (Emer: col. 3, lines 33-59).

For claim 12, the combined teachings of Hironaka and Emer as per rejection of claim 10 further help disclose each said bank of said first cache contains a plurality of read ports and at least one write port (Hironaka: par. 0131, 0146, 0028).

For claim 18, the combined teachings of Hironaka and Emer as per rejection of claim 10 further help disclose said computer system comprises a plurality of caches at different cache levels, said first cache being at a level closest said processor (Emer: a first memory for storing data, and a second memory, relatively smaller and faster than the first memory, for storing a subset of the data from the first memory, where the second memory is apportioned into a plurality of banks, and each of said banks has a plurality of locations for storing data; a third memory having a plurality of locations, each of the locations associated with one of the locations of the second memory, where each of the locations of the third memory stores a prediction value, col. 3, lines 47-56).

For claim 19, the combined teachings of Hironaka and Emer as per rejection of claim 10 further help disclose said computer system comprises a plurality of said processors, each processor being coupled to a respective first cache, and wherein said bank predict values associated with instructions are maintained in a location accessible to each of said plurality of processors (Hironaka: a parallel processor which executes a plurality of types of processing in one clock cycle as typified by a super scalar processor has come into practical use, par. 0007; where it would have been obvious to one of

ordinary skill in the art at the time of the application that a plurality of processors could be used).

For claim 20, the combined teachings of Hironaka and Emer as per rejection of claim 10 are incorporated herein.

These teachings further help disclose a digital data processing device, comprising:

a cache for temporarily storing data, said cache comprising a plurality of banks, each bank containing at least one respective access port for accessing data in the bank (Hironaka: par. 0131);

execution logic for executing multiple instructions concurrently (Hironaka: par. 0132);

instruction logic for selecting and dispatching, in each of multiple execution dispatch cycles, a respective subset of instructions for concurrent execution, each said subset of instructions being selected from among a respective set of instructions eligible for execution dispatch, wherein for at least some said respective sets of instructions eligible for execution dispatch, the corresponding subset of instructions selected for concurrent execution is smaller than the respective set of instructions eligible for execution dispatch, wherein at least some said instructions access said cache, said instruction logic using a respective bank predict value associated with at least some instructions accessing said cache select instructions for inclusion in said subsets by predicting whether multiple instructions accessing said cache can be concurrently executed without conflict by said processing device, each respective said bank predict

value predicting a bank of said cache to be access by its associated instruction (Emer: abstract; col. 3, lines 33-59; Hironaka: 0203, 0131-0132, 0146; a multi-port cache has a plurality of banks white store parts of instructions and a plurality of ports, and executes a plurality of types of processing in one clock cycle, par. 0049).

6. Claims 4-8 and 13-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hironaka et al (US PGPub No. 20040088489), Emer et al (US Patent No. 5,933,860) and Winberg et al (US PGPub No. 20040199752).

For claim 4, the combined teachings of Hironaka and Emer disclose the invention as per rejection of claim 1 above.

These teachings fail to disclose a respective confirmation value is associated with each said instruction with which a bank predict value is associated, each confirmation value reflecting a degree of confidence in the respective bank predict value.

Winberg helps disclose a load value prediction unit comprises a load classification table for deciding which predictions are likely to be correct, wherein the table includes counters for load instructions which indicate the success rate of previous predictions and are incremented for correct predictions and decremented others; based on the value of the counter a load instruction is classified as unpredictable, predictable or constant (par. 0008).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to combine Hironaka, Emer and Winberg to include a confirmation value

for reflecting a degree of confidence in a respective bank predict value because this would help in deciding whether or not to execute instructions speculatively based on a predicted value (par. 0011), as taught by Winberg.

For claim 5, the combined teachings of Hironaka, Emer and Winberg as per rejection of claim 4 further help disclose said digital data processing device dynamically maintains said confirmation values (Winberg: par. 0008).

For claim 6, the combined teachings of Hironaka, Emer and Winberg as per rejection of claim 5 further help disclose each said confirmation value is a counter which is incremented for each correct bank prediction and decremented for each incorrect bank prediction (Winberg: par. 0008).

For claim 7, the combined teachings of Hironaka, Emer and Winberg as per rejection of claims 1 and 6 further help disclose feedback logic which maintains bank prediction history data in a form accessible to a programmer, said bank prediction history data recording the performance of bank predictions by said bank predict values during execution of a computer program (Winberg: par. 0008).

For claim 8, said instruction logic concurrently selects and decodes instructions for execution from a plurality of threads (Hironaka: par. 0203, 0131, 0146).

For claim 13, the combined teachings of Hironaka, Emer and Winberg as per rejection of claims 4 and 10 further help disclose a respective confirmation value is associated with each said instruction with which a bank predict value is associated, each confirmation value reflecting a degree of confidence in the respective bank predict value (Winberg: par. 0008).

For claim 14, the combined teachings of Hironaka, Emer and Winberg as per rejection of claims 5 and 10 further help disclose said computer system dynamically maintains said confirmation values (Winberg: par. 0008).

For claim 15, the combined teachings of Hironaka, Emer and Winberg as per rejection of claims 6 and 10 further help disclose each said confirmation value is a counter which is incremented for each correct bank prediction and decremented for each incorrect bank prediction (Winberg: par. 0008).

For claim 16, the combined teachings of Hironaka, Emer and Winberg as per rejection of claims 7 and 10 further help disclose feedback logic which maintains bank prediction history data in a form accessible to a programmer, said bank prediction history data recording the performance of bank predictions by said bank predict values during execution of a computer program (Winberg: par. 0008).

For claim 17, the combined teachings of Hironaka, Emer and Winberg as per rejection of claims 8 and 10 further help disclose said instruction logic concurrently selects and decodes instructions for execution from a plurality of threads (Hironaka: par. 0203, 0131, 0146).

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Citation of Pertinent Prior Art

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Nakamura (US PGPub No. 20020152368) discloses an instruction cache to store instructions to which a value prediction field is attached.

Contact Information

9. Any inquiries concerning this action or earlier actions from the examiner should be directed to Daniel Kim, reachable at 571-272-2742, on Mon-Fri from 10:00am-6:30pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah, is also reachable at 571-272-4098.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information from

published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. All questions regarding access to the Private PAIR system should be directed to the Electronic Business Center (EBC), reachable at 866-217-9197.

DK

10-6-06

SCElmore 10/12/06
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